Product Information

To:

Product Name: C043GW32 R1

Document Issue Date: 2015/10/14

Customer	InfoVision Optoelectronics
SIGNATURE _____ _____ _____ **Please return 1 copy for your confirmation with your signature and comments.**	**SIGNATURE** **REVIEWED BY** **QA** _____ **PREPARED BY** **FAE** _____

Note: 1. Please contact InfoVision Company. before designing your product based on this product.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by IVO for any intellectual property claims or other problems that may result from application based on the module described herein.

CONTENTS

1 General Descriptions

1.1 Introduction

The C043GW32 R0 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) Single Chip and Sub Chips that uses amorphous silicon TFT as a switching device. This TFT LCD panel has a 4.3-inch diagonally measured active display area with WQVGA resolution (480 horizontal by 272 vertical pixels array).

1.2 Features

- 4.3” TFT-LCD Panel
- Supported WQVGA Resolution
- Compatible with ROHS Standard

2 General Characteristics

Item	Specification	Unit	Note
Screen Diagonal	4.3	inch	-
Active Area (H x V)	95.04 x 53.856	mm	Single Chip
Number of Pixels (H x V)	480 x 272	-	Single Chip
Pixel Size (H x V)	0.198 x 0.198	mm	Single Chip
Outline Dimension (H x V x D)	102.04(Typ.) x 63.006(Typ.) x 1.0(Typ.)	mm	Single Chip
Display Type	Transmissive	-	-
Display Mode	Normally White	-	-
Response Time	(16) (Typ.) (25) (Max)	ms	-
Contrast Ratio	(500) (Typ.) (400) (Min)	-	-
Viewing Angle (Left/Right/Up/Down)	(75/75/60/70) (typ) (65/65/50/60) (min)	deg.	-
NTSC	(50) (Typ.)	%	-
Transmittance	(6.0)(Typ.)	%	Under C-light
Pixel Arrangement	R.G.B. Stripe	-	-
Weight	(15.71) (Max.)	g	Single Chip
	(861) (Max.)	g	Sub Chips

3 Absolute Maximum Ratings

Table 2 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	(-20)	(70)	℃	(1),(2)
Operating Humidity	HOP	(10)	(85)	%RH	
Storage Temperature	TST	(-30)	(80)	℃	
Storage Humidity	HST	(10)	(90)	%RH	

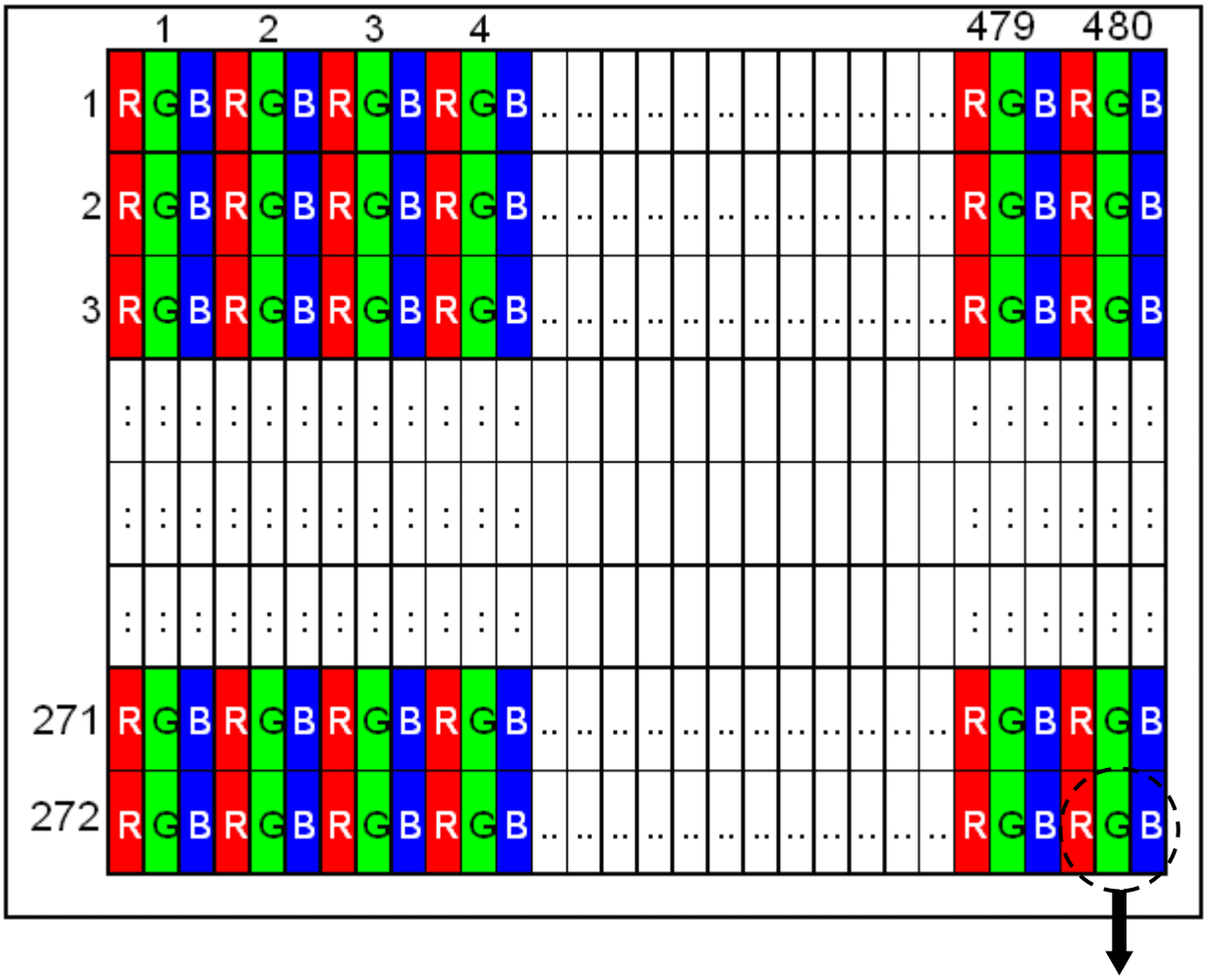
Note (1) Maximum Wet-Bulb should be 39 ℃. No condensation.

(2) When you apply the LCD panel for OA system. Please make sure to keep the temperature of LCD panel is less than 70℃.

4 Pixel Format

The figure shows the relationship of the input signals and LCD panel pixel format.

Figure 3 Pixel Format



5 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

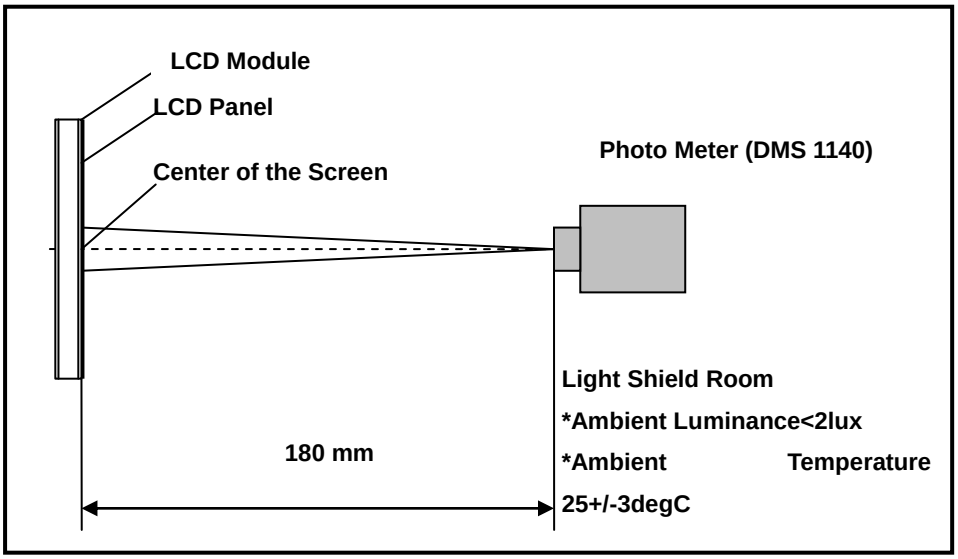
Table 3 Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle （CR>10）	Horizontal	θ_{x+}	(65)	(75)	-	degree	(1),(2),(6),(7),(8)
		θ_{x-}	(65)	(75)	-		
	Vertical	θ_{y+}	(50)	(60)	-		
		θ_{y-}	(60)	(70)	-		
Contrast Ratio	Center		(400)	(500)	-	-	(1),(3),(6)(7),(8)
Response Time	Rising + Falling		-	(16)	(25)	ms	(1),(4),(6),(7),(8)
CF Color Chromaticity (CIE1931)	Red x		Typ.-0.03	(0.604)	Typ.+0.03	-	Under C-light
	Red y			(0.329)		-	
	Green x			(0.293)		-	
	Green y			(0.552)		-	
	Blue x			(0.147)		-	
	Blue y			(0.140)		-	
	White x		Typ.-0.03	(0.310)	Typ.+0.03	-	
	White y			(0.337)		-	
NTSC	CIE1931		-	(50)	-	%	(1),(6),(7),(8)
Transmittance	-		-	(6.0)	-	%	Under C-light (1),(5),(6),(7),(8)

Note (1) Measurement Setup:

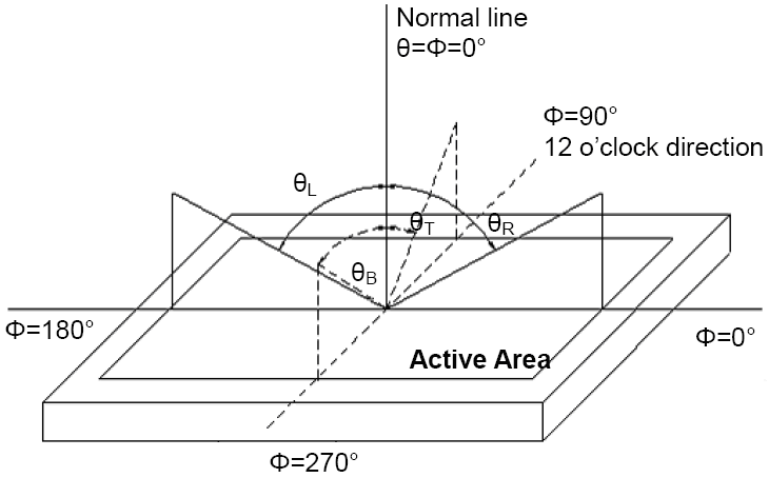
The LCD module should be stabilized at given temperature(25°C) for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

Figure 1 Measurement Setup



Note (2) Definition of Viewing Angle

Figure 2 Definition of Viewing Angle



Note (3) Definition Of Contrast Ratio (CR)

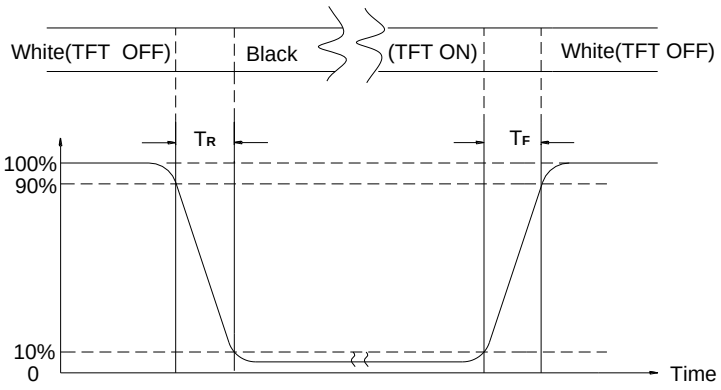
The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note (4) Definition Of Response Time

Figure 3 Definition of Response Time

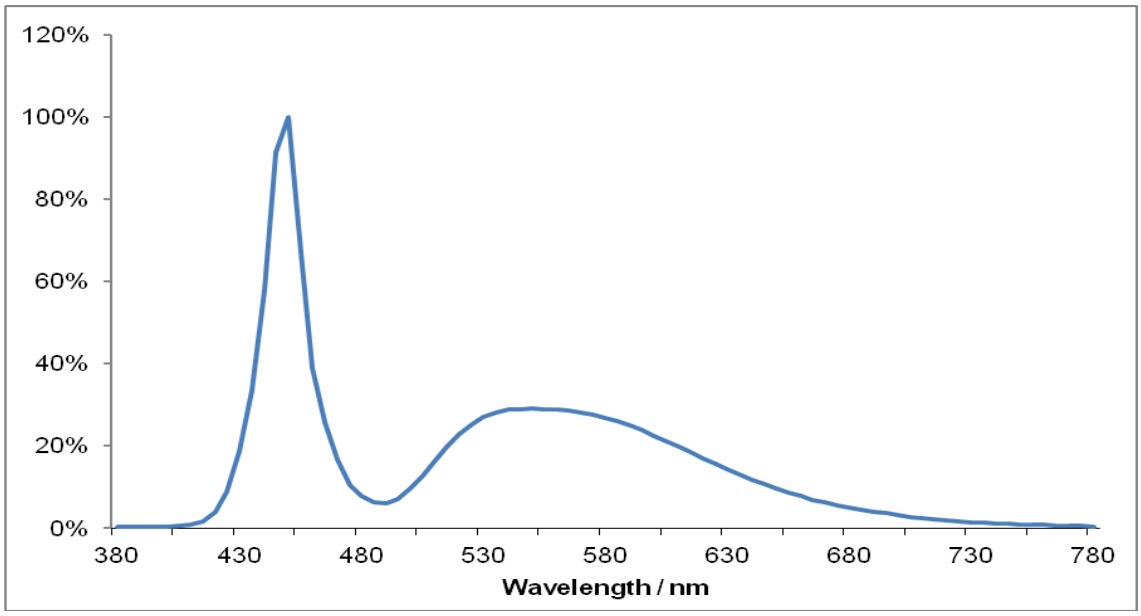


Note (5) Definition of Transmittance

$$\text{Transmittance} = \frac{\text{Center Luminance of LCD}}{\text{Center Luminance of Back Light}} \text{ X100\%}$$

Note (6) Light source is the BLU which is supplied by IVO.

Figure 4 Back Light Spectrum

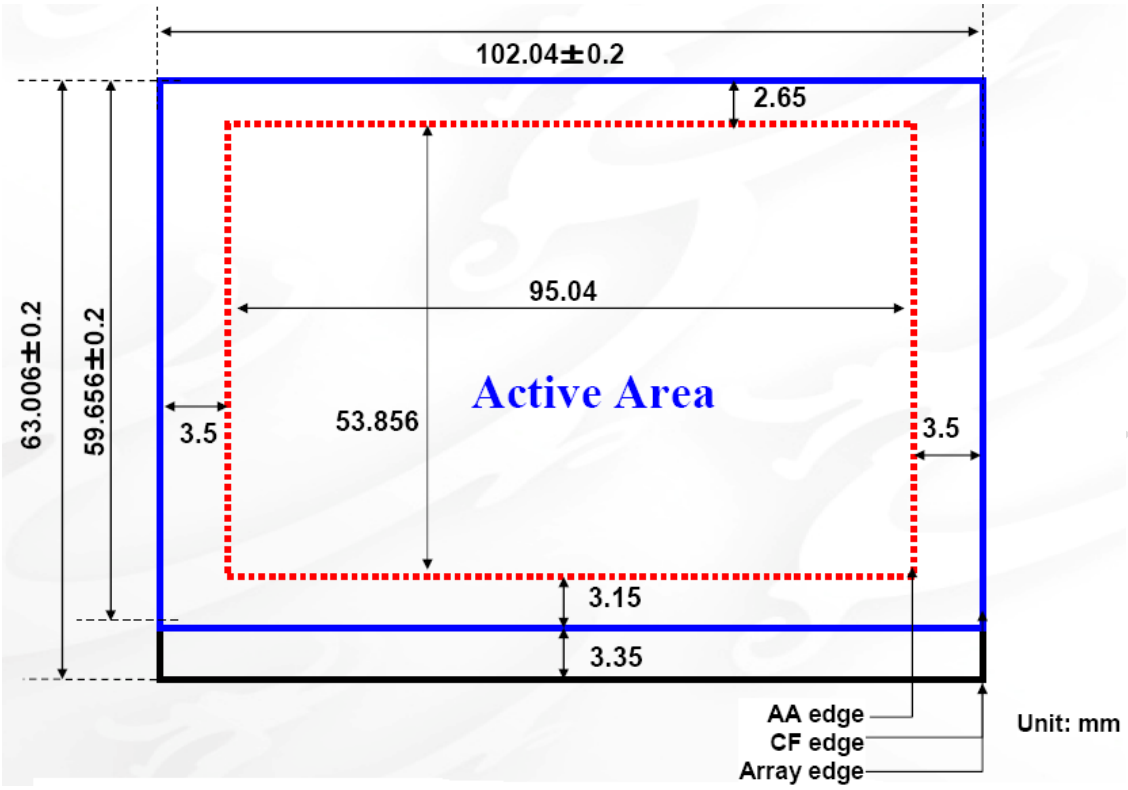


Note (7) The polarizer manufacturer: LG;
Type: XT320G0432R0IVOT/CF; XT300G0432R0IVOB/Array.

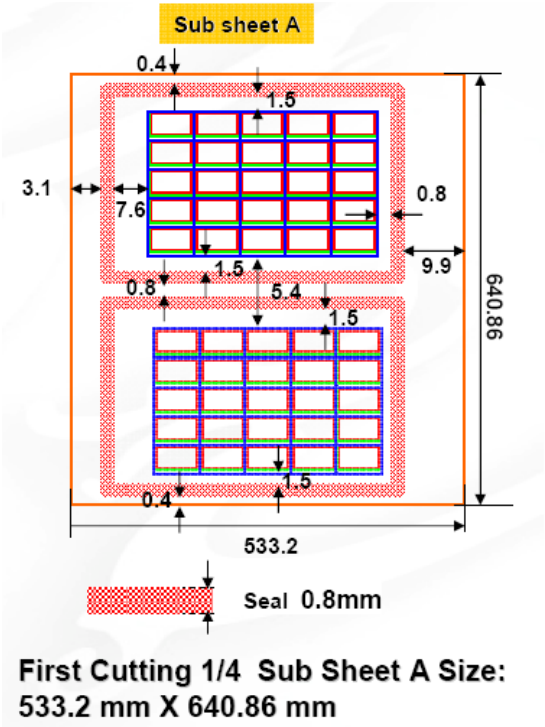
Note (8) All optical data based on IVO given polarizer & Backlight& testing machine in this document.

6 Cell Outline Size

6.1 Outline Size of Single Chip



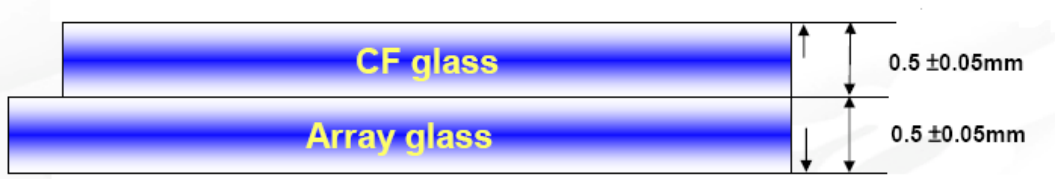
6.2 Outline Size of Sub Chips and Cut Mark



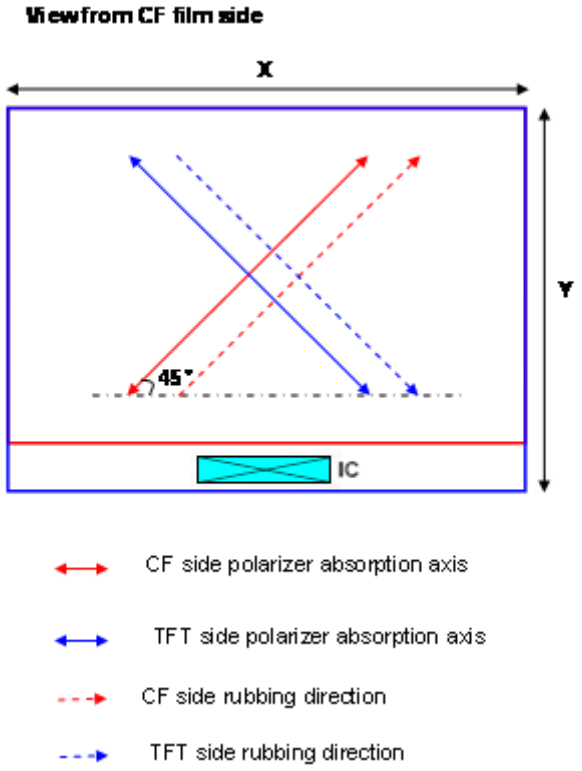
First Cutting 1/4 Sub Sheet A Size:
533.2 mm X 640.86 mm

7 Cell Thickness

7.1 Thickness of Single Chip

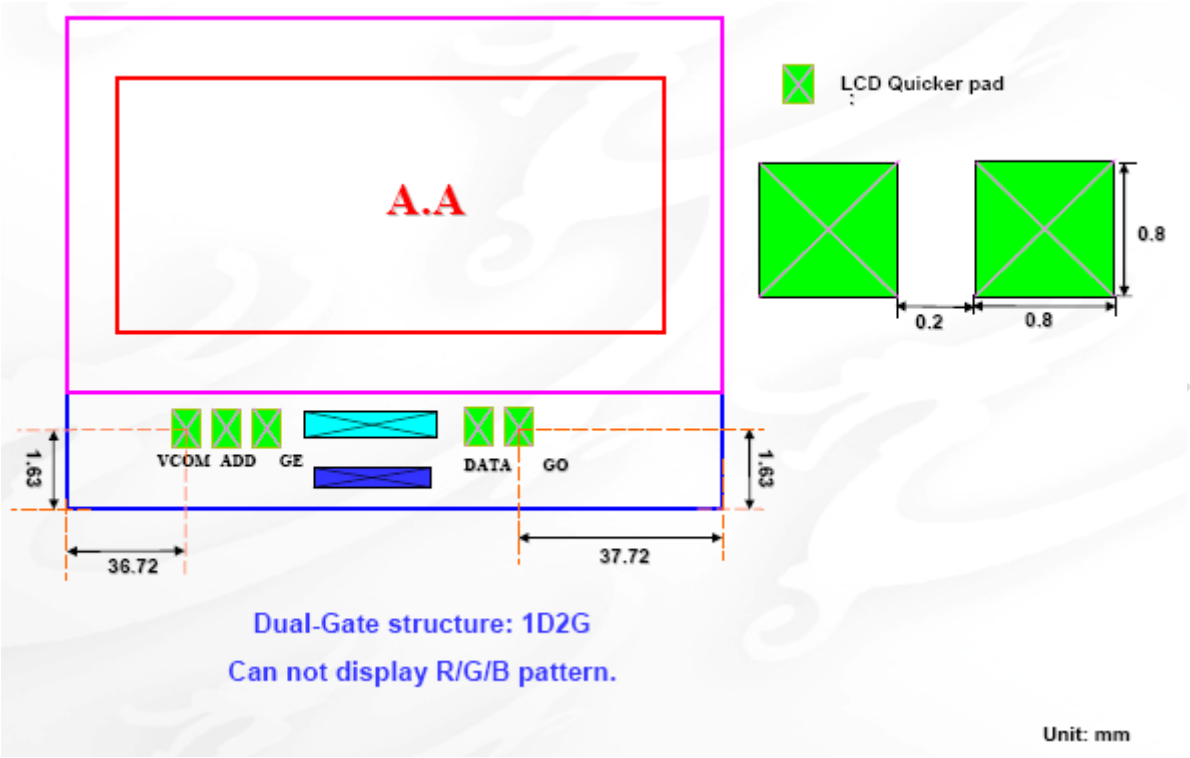


8 CF/Array Side Rubbing Direction

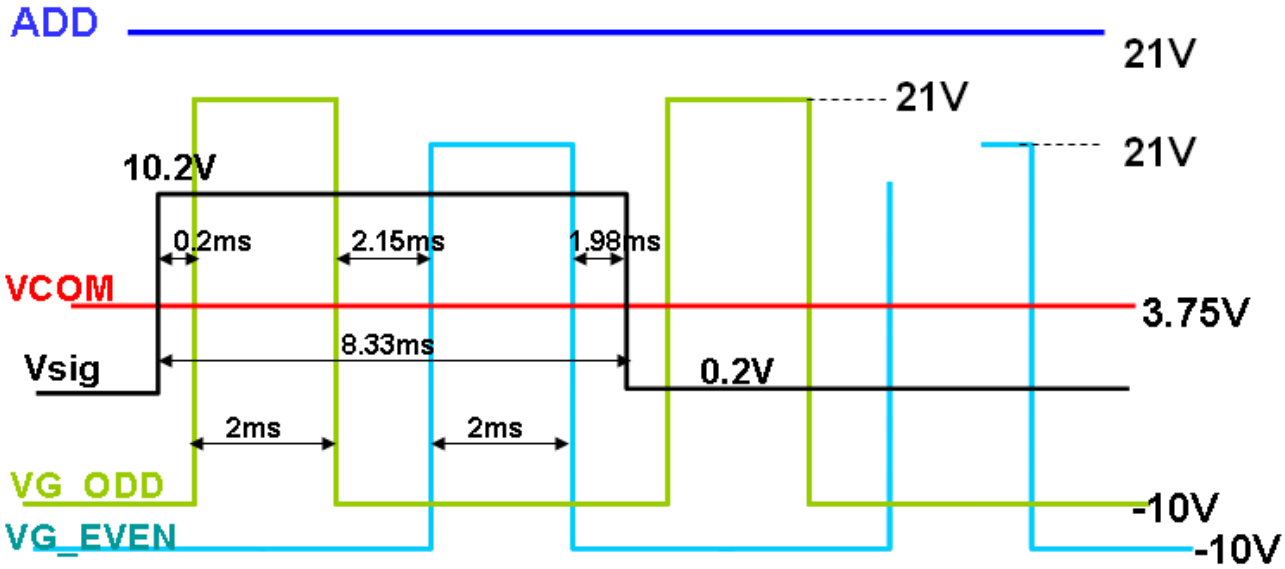


9 Cell Light-On Information

9.1 Cell Light-On Test Pad Drawing



9.2 Cell Light-On Test Waveform

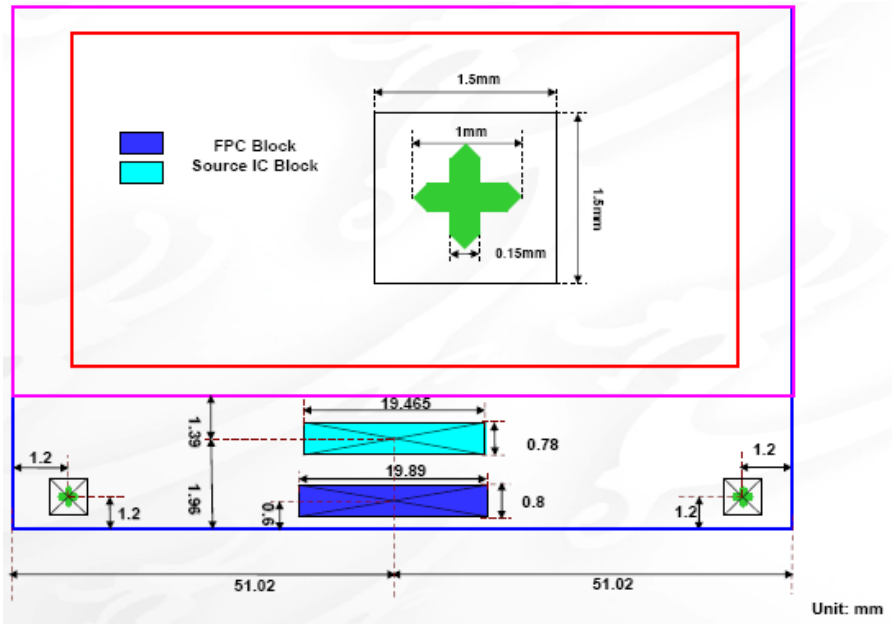


9.3 Vdata Voltage Table

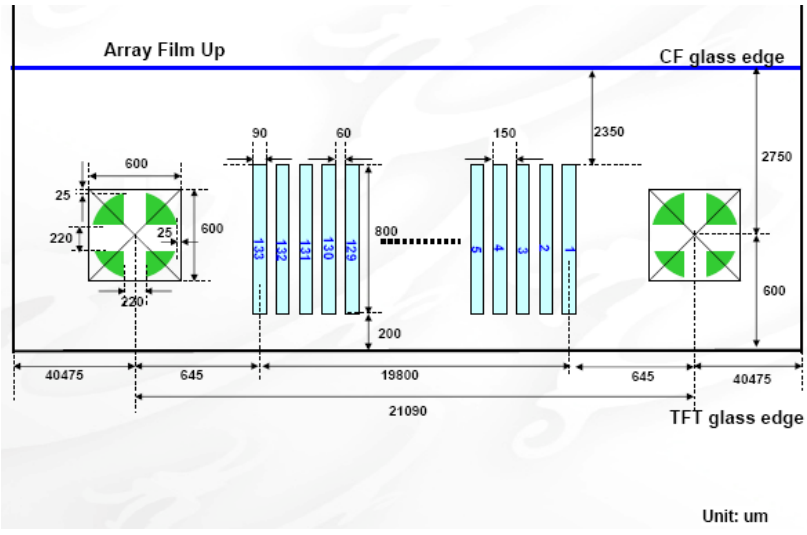
Display Pattern	V_{sig}	VGO	VGE	Vcom	ADD	Unit
Black	(10.2)	(21)	(21)	(3.75)	(21)	V

	(0.2)	(-10)	(-10)			V
Gray	(7.2)	(21)	(21)	(3.75)	(21)	V
	(3.2)	(-10)	(-10)			V
White	(5.4)	(21)	(21)	(3.75)	(21)	V
	(5)	(-10)	(-10)			V

10 Source COG/FPC Position On Cell

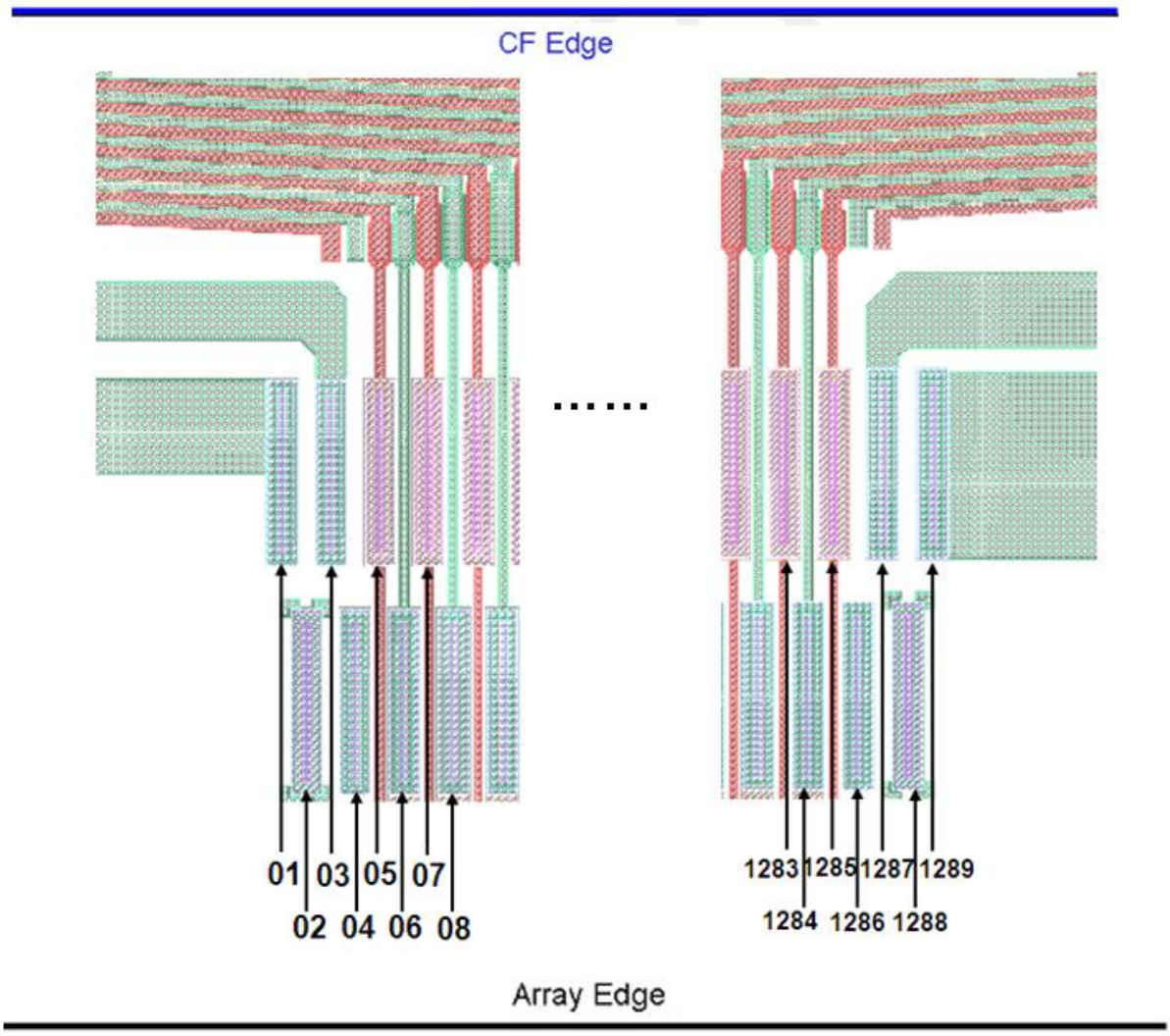


11 FPC Pad Information



12 Cell Electrode Pin Assignment

12.1 Source Pad Pin Assignment



Pad ID	Array side
01	Through 5
02	Dummy
03	Through 6
04	Dummy
05	Gate 2
06	Gate 4
07	Gate 6
08	Gate 8
…	…
274	Gate 540
275	Gate 542
276	Gate 544
277	Dummy
278	PRT4

279	PRT3
280	PRT2
281	PRT1
282	Dummy
283	Date 1
284	Date 2
285	Date 3
...	…
640	Date 358
641	Date 359
642	Date 360
643	Dummy
644	Dummy
645	Dummy
646	Dummy
647	Dummy
648	Date 361
649	Date 362
650	Date 363
…	…
1005	Date 718
1006	Date 719
1007	Date 720
1008	Dummy
1009	PLT1
1010	PLT2
1011	PLT3
1012	PLT4
1013	Dummy
1014	Gate 543
1015	Gate 541
1016	Gate 539
…	…
1283	Gate 5
1284	Gate 3
1285	Gate 1
1286	Dummy
1287	Through 7
1288	Dummy
1289	Through 8

12.3 FPC Pin Assignment

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	DUMMY	35	C3P	69	EXVR	103	D20
2	DUMMY	36	C3P	70	VSSRC	104	D21
3	VCOM	37	C3N	71	VSSRC	105	D22
4	VFB2	38	C3N	72	VDD	106	D23
5	VFB1	39	C4N	73	VDD	107	D24
6	COML	40	C4N	74	VCI	108	D25
7	COML	41	DUMMY	75	VCI	109	D26
8	COMH	42	VGL	76	VCI	110	D27
9	COMH	43	VGL	77	VCIP	111	DUMMY
10	COMC	44	DUMMY	78	VCIP	112	CLK
11	COMPP	45	PSW	79	VDDIO	113	DISP
12	VGR	46	PSW	80	VDDIO	114	HS
13	C5P	47	VCHS	81	DVSS	115	VS
14	C5P	48	VCHS	82	DVSS	116	DE
15	C5N	49	VCHS	83	PSHUT	117	UD
16	C5N	50	AVSS	84	POL	118	LR
17	VCL	51	AVSS	85	RESETB	119	CLK_TRG
18	VCL	52	AVSS	86	D00	120	PS
19	DUMMY	53	VDC	87	D01	121	CSB
20	VGH	54	VDC	88	D02	122	SCL
21	VGH	55	VCIX2J	89	D03	123	SDI
22	DUMMY	56	VCIX2J	90	D04	124	SDO
23	C2P	57	VCIX2	91	D05	125	NBW
24	C2P	58	VCIX2	92	D06	126	DVSS
25	C1AP	59	CX2N	93	D07	127	DVSS
26	C1AP	60	CX2N	94	DUMMY	128	DVSS
27	C1BP	61	CX2P	95	D10	129	RES
28	C1BP	62	CX2P	96	D11	130	DUMMY
29	C1N	63	CX1N	97	D12	131	VCOM
30	C1N	64	CX1N	98	D13	132	DUMMY
31	C2N	65	CX1P	99	D14	133	DUMMY
32	C2N	66	CX1P	100	D15		
33	C4P	67	VLCD	101	D16		
34	C4P	68	VLCD	102	D17		

12.4 FPC Pin Assignment Description

No.	Pin Assignment	Description
1~2	DUMMY	Dummy pin. Floating it on panel.
3	VCOM	Output pin for COMMON signal of a TFT panel.
4	VFB2	Main boost regulator feedback input 2. Connect feedback resistive divider to GND, If 2nd PWM is not used, please connect VFB2 to GND. VFB2 default threshold is 1.0V.
5	VFB1	Main boost regulator feedback input 1. Connect feedback resistive divider to GND, If 1st PWM is not used, please connect VFB1 to GND. VFB1 default threshold is 1.0V.
6~7	COML	output pin of regulator for COMMON output low level.
8~9	COMH	output pin of regulator for COMMON output high level.
10	COMC	Adjust the DC voltage level for COMMON output. If not used, please leave it open.
11	COMPP	Adjust the amplitude voltage level for COMMON output. If not used, please leave it open.
12	VGR	Output pin of internal regulator circuit.
13~14	C5P	Connect 0.1uF capacitor between CnP and CnN pins.
15~16	C5N	
17~18	VCL	Negative voltage of VCI. Connect a capacitor for stabilization.
19	DUMMY	Dummy pin. Floating it on panel.
20~21	VGH	Positive power pin for gate driver.
22	DUMMY	Dummy pin. Floating it on panel.
23~24	C2P	Connect 0.1uF capacitor between CnP and CnN pins.
25~26	C1AP	
27~28	C1BP	
29~30	C1N	
31~32	C2N	
33~34	C4P	
35~36	C3P	
37~38	C3N	
39~40	C4N	
41	DUMMY	Dummy pin. Floating it on panel.
42~43	VGL	Negative power pin for gate driver.
44	DUMMY	Dummy pin. Floating it on panel.
45~46	PSW	Internal switch input. This is used only for 2nd PWM(PEM B). If 2nd PWM id not used, please leave it open
47~49	VCHS	Ground for booster circuit.
50~52	AVSS	Analog ground.
53~54	VDC	Power for reference voltage of VGH/VGL pumping.

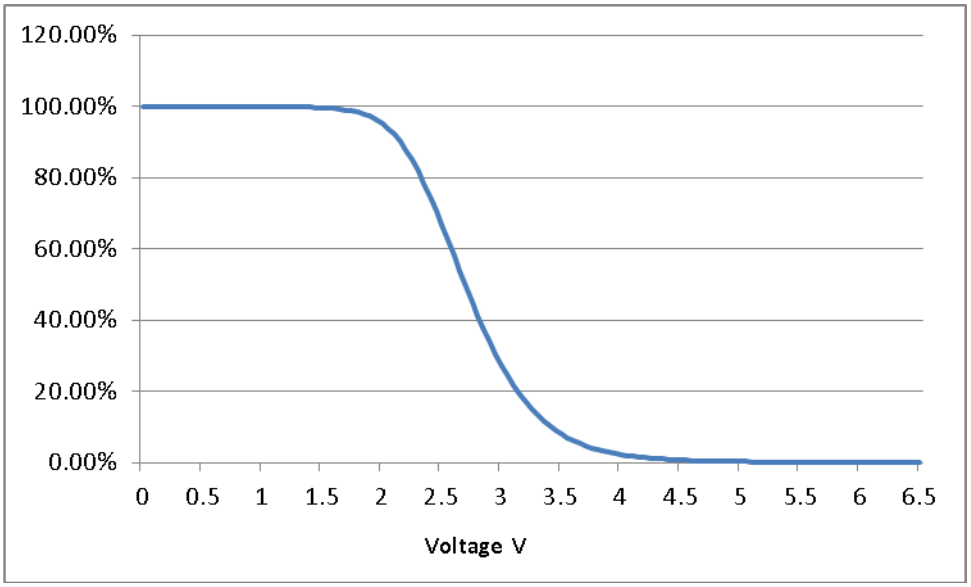
55~56	VCIX2J	This is the power supply used for analog blocks and VLCD/VDC regulation.
57~58	VCIX2	Equal to 2*VCI. Connect a capacitor for stabilization.
59~60	CX2N	Connect 0.1uF capacitor between CnP and CnN pins.
61~62	CX2P	
63~64	CX1N	
65~66	CX1P	
67~68	VLCD	Internal generated power for gamma circuit. Connect a capacitor for stabilization.
69	EXVR	External reference of internal gamma resistor.
70~71	VSSRC	Ground for analog circuit. This pin requires a noise free path for providing accurcate LCD driving voltages.
72~73	VDD	Inernal regulator output voltage for logic circuit. Connect a capacitor for stabilization.
74~76	VCI	Booster input voltage pin.
77~78	VCIP	Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. Can be connected to VCI on system borad or FPC.
79~80	VDDIO	Voltage input pin fot I/O logic.
81~82	DVSS	Digital ground.
83	PSHUT	Input pin to enable internal charge pump circuit. Internal pull high. -Connect to VDDIO to enable internal charge pump VCL,VGH,VGL,VCIX2 and VCOM. -Connect to DVSS to disable internal charge pump VCL,VGH,VGL,VCIX2 and VCOM.
84	POL	Polatity signal to monitor VCOM signal.
85	RESETB	Active low global reset signal input. Internally pulled high.
86	D00	Digital data input. Internally pulled low.
87	D01	
88	D02	
89	D03	
90	D04	
91	D05	
92	D06	
93	D07	
94	DUMMY	Dummy pin. Floating it on panel.
95	D10	Digital data input. Internally pulled low.
96	D11	
97	D12	
98	D13	
99	D14	

100	D15	
101	D16	
102	D17	
103	D20	
104	D21	
105	D22	
106	D23	
107	D24	
108	D25	
109	D26	
110	D27	
111	DUMMY	Dummy pin. Floating it on panel.
112	CLK	Clock signal for data latching and internal counter of the timing controller.
113	DISP	Dispay on/off mode control. Internally pulled high. DISP=L, standby mode. DISP=H, normal display mode.
114	HS	Horizontal sync input with negative polarity. Inernally pull high.
115	VS	Vertical sync input with negative polarity. Internally pull high.
116	DE	Input data enable control. Internally pulled low.
117	UD	Scan direction selection signal. Inrternally pulled high. UD=H:G1→G2→...→G544 UD=L:G544→G543→...→G1
118	LR	Shift direction selection signal. Internally pulled high. Shift direction of the internal shift register is controlled by this pin sa shown below. LR=H:S1→S2→...→S720 LR=L:S720→S719→...→S1
119	CLK_TRG	Clock edge selection signal for the data sampling. Internally pulled high. CLK_TRG=H:Data samping at the CLK falling edge. CLK_TRG=L:Data samping at the CLK rising edge.
120	PS	Input data format select signal. Internally pulled high. PS=H: Paralled RGB PS=L: Serial RGB
121	CSB	Chip select pin of serial interface. Internal pull high.Leave it open when not used.
122	SCL	Clock pin of serial interface.Internal pull high.Leave it open when not used.
123	SDI	Data input pin in serial mode.Internal pull high.Leave it open when not used.
124	SDO	Data output pin in serial mode.Leave it open when not used.
125	NBW	LC type selection. Internally pulled high.

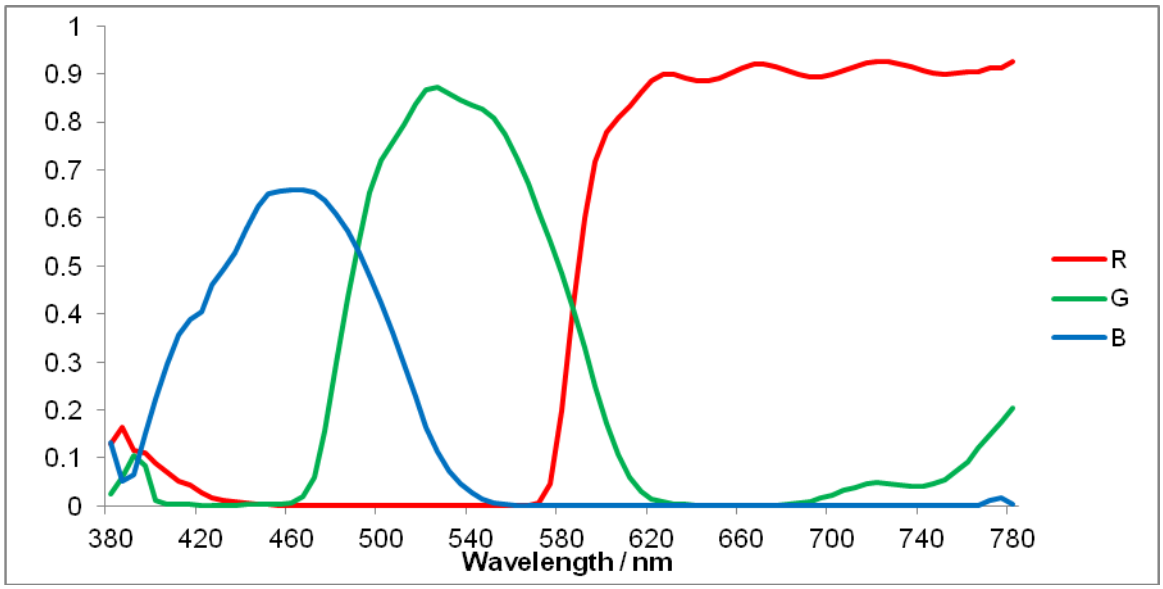
		NBW=H: Normally black LC NBW=L: Normally white LC
126~128	DVSS	Digital ground.
129	RES	Resolution select signal. Internally pulled high. RES=H: 480RGBX272 RES=L: 480RGBX240
130	DUMMY	Dummy pin. Floating it on panel.
131	VCOM	Output pin for COMMON signal of a TFT panel.
132~133	DUMMY	Dummy pin. Floating it on panel.

13 V-T Curve

13.1 V-T Curve (Reference)



13.2 CF Spectrum (Reference)



Note:. Measured at ambient temperature 23ºC , under C-light condition.

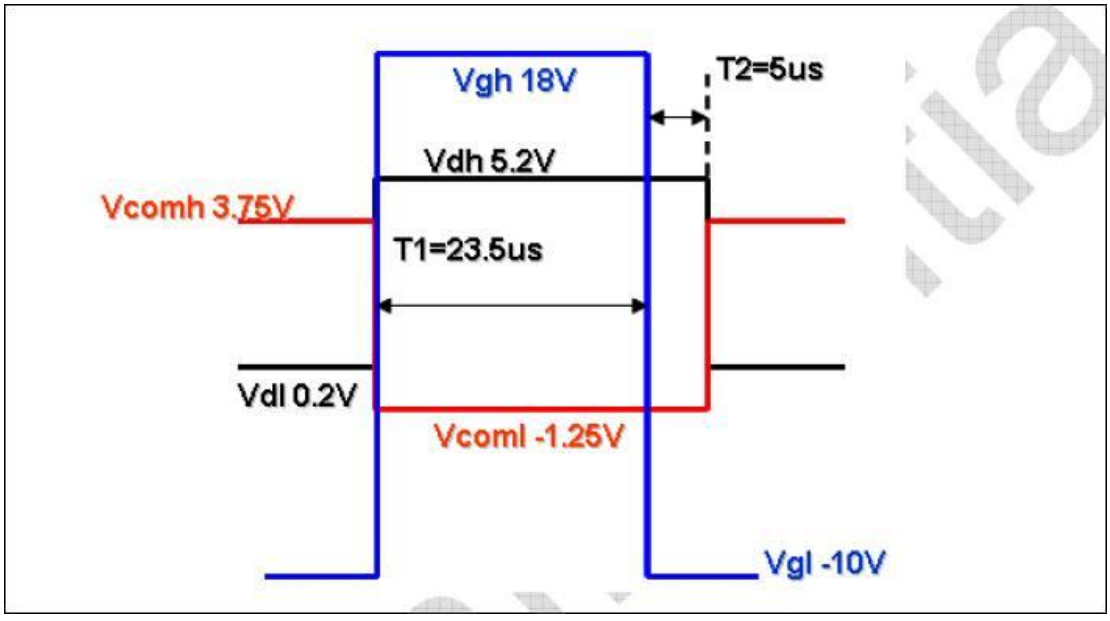
14 IVO Requirement Driving Condition

14.1 Timing Range (Reference)

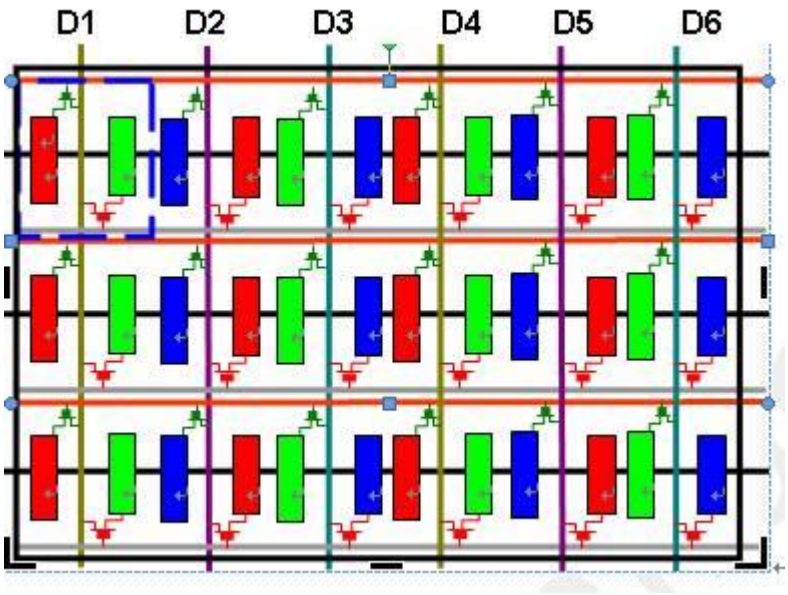
Category	Parameter	Unit	Min.	Typ.	Max.
Timings	Frame Rate	Hz	-	(60)	-
Scanning Method	Gate Scanning Method (Single / Double)	Dual gate			
Line Impedance	Capacitive Load of a Signal Line	pF	-	(3.935)	-
	Capacitive Load of a Gate Line	pF	-	(72.345)	-
	Resistance Load of Signal Line	KOhm	-	(2.394)	-
	Resistance Load of Gate Line	KOhm	-	(2.232)	-

14.2 Power Supply Voltage (Reference)

No.	Item	Min.	Typ.	Max.	Unit
1	Vcom_H voltage	(3.6)	(3.75)	(3.9)	V
2	Vcom_L voltage	(-1.4)	(-1.25)	(-1.1)	V
3	Vgl voltage	(-11)	(-10)	(-9)	V
4	Vgh1 voltage	(17)	(18)	(19)	V
5	Vgh2 voltage	(17)	(18)	(19)	V
6	Vdl voltage	-	(0.2)	-	V
7	Vdh voltage	-	(5.2)	-	V
8	Gata line charging time [T1]	-	(23.5)	-	us
9	Data line delay closing time [T2]		(5)		us
10	2Line=2x(T1+T2)	-	(57)	-	us



14.3 Panel Driving Condition



14.4 Gamma Reference Voltage

TBD

14.5 OLB Information

Item	Driver
Output Channels	1264
Driver Amount	1
Component Type	COG
OLB Pad Pitch	30um

14.6 Driver Recommendation

Source Driver Supplier	Himax
Source Driver Model	HX8257-A01

15 Reliability test items

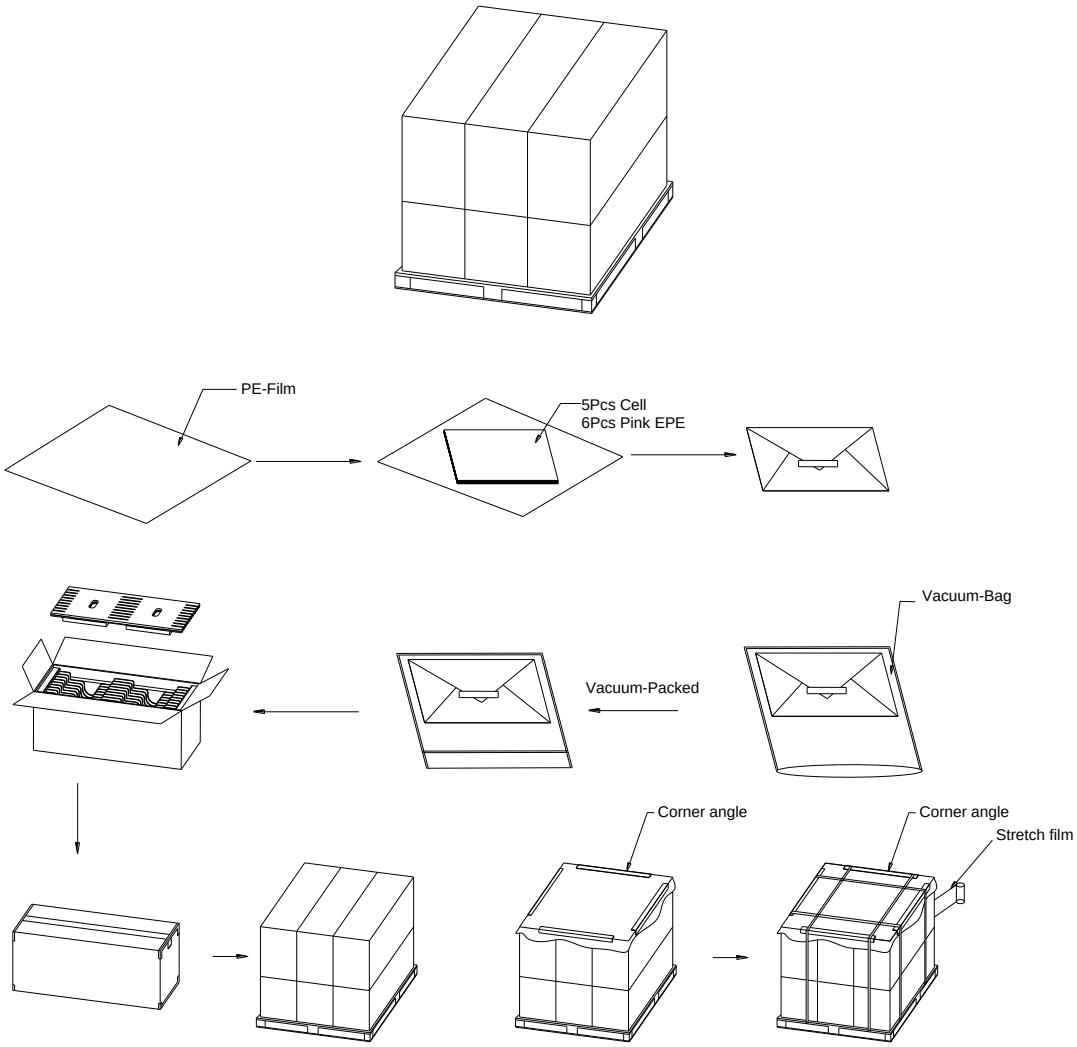
No.	Item	Conditions	Note
1	High Temperature Storage	Ta=+80℃,240hrs	(1),(2)
2	Low Temperature Storage	Ta=-30℃,240hrs	
3	High Temperature Operation	Ta=+70℃,240hrs	
4	Low Temperature Operation	Ta=-20℃,240hrs	
5	High Temperature and High Humidity (Operating)	Ta=+50℃, 90%RH,240hrs	

Note: (1) All tests above are practiced at module type.

(2) There is no display function NG issue occurred, all the cosmetic specification is judged before the reliability stress.

16 IVO Recommended Cell Packaging

16.1 Sub 50 Chips Packaging



17 General Precaution

17.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

17.2 Handling Precaution

(1) Since the LCD panel is made of glass, do not apply strong mechanical impact or static load onto it. Handling with care since shock, vibration, and careless handling may seriously affect the product. If it fall a high place or receives a strong shock, the glass maybe broken.

(2) Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD for incoming inspection or assembly.

(3) When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

(4) Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

(5) When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

17.3 Storage Precaution

(1) Please do not leave cell in the environment of high humidity and high temperature for long time.

(2) IVO suggests to assembly the panel to LCD module in one month after cut into single chip.

(3) The cell should be stored in a dark place .Store in an ambient temperature of 5°C to 45°C,and in a relative humidity of 40%RH to 60%RH.Don't expose to sunlight or fluorescent light.

(4) Storage in a clean environment, free from dust, active gas, and solvent.

(5) Store in anti-static electricity container.

(6) Store without any physical load.

17.4 Caution For Operation

(1) The polarizer on the surface of panel are made from organic substance. Be very careful for chemicals not to touch the polarizer or it leads the polarizer to be deteriorated.

(2) Dot drop water or any chemicals onto the LCD panel surface.

(3) Please do not leave LCD panel in the environment of high humidity and high temperature for a long time.

(4) Do not connect or disconnect the LCD panel to or from the system when power is on.

(5) When expose to drastic fluctuation of temperature(hot to cold or cold to hot），the LCD panel may be affected; specifically, drastic temperature fluctuation from cold to hot, produces dew on the LCD panel surface which may affect the operation of the polarizer and the LCD panel.

(6) Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD panel structure.

(7) The temperature of baking should be under 85℃.

17.5 Static Electricity

(1) Protection film must remove very slowly from the surface of LCD panel to prevent from electrostatic occurrence if the LCD panel attaches a polarizer.

(2) Because TFT-LCD panel is very weak to electrostatic discharge, please be careful with electrostatic discharge. Persons who handle the LCD panel should be grounded through adequate methods.

17.6 Safety

(1) For the crash damaged or unnecessary LCD panel, it is recommended to wash off liquid crystal
by either of solvents such as acetone and ethanol an should be burned up later.

(2) In the case the LCD panel is broken, watch out whether liquid crystal leaks out or not. If your hands touch the liquid crystal, wash your hands cleanly with water an soap as soon as possible.

(3) If you should swallow the liquid crystal, first, wash your mouth thoroughly with water, then drink a lot of water and induce vomiting, and then, consult a physician.

(4) If the liquid crystal should get in your eyes, flush your eyes with running water for at least fifteen minutes.

(5) If the liquid crystal touches your skin or clothes, remove it and wash the affected part of your

skin or clothes with soap and running water.

17.7 Disposal

When disposing LCD panel, obey the local environmental regulations.